WHAT IS CLAIMED IS:

1. A delay analysis system for making a delay analysis of a logic circuit,

said system having a delay analysis library containing connection information on a plurality of circuits and delay time information on rises and falls of each input terminal and output terminal of said plurality of circuits,

wherein said library further contains logical operation information representing correspondence between a logical value of each input terminal and the logical value of the output terminal of said plurality of circuits, and

wherein, when making a delay analysis of the logic circuit including at least one of said plurality of circuits, a delay time between the input terminal and the output terminal is selected, according to a logical operation of said at least one of circuits, from the delay time information on the rises and falls of the input and output terminals of said plurality of circuits for use in delay calculation, said logical operation being specified by said logical operation information, said delay time information being stored in said library, and delay calculation is performed.

2. A delay analysis system for making a delay analysis of a logic circuit, said system having a delay analysis library

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containing connection information on a plurality of circuits and delay time information on rises and falls of each input terminal and output terminal of said plurality of circuits,

wherein said library further contains logical operation information representing correspondence between a logical value of each input terminal and the logical value of the output terminal of said plurality of circuits, and

wherein, when making a delay analysis of the logic circuit, a delay time between the input terminal and the output terminal is selected, according to a logical operation of said circuits, from the delay time information on the rises and falls of the input and output terminals of said plurality of circuits for use in delay calculation, said logical operation being specified by said logical operation information, said delay time information being stored in said library, and delay calculation is performed.

3. A method for making a delay analysis of a logic circuit, comprising the steps of:

referencing as library information a delay analysis library containing connection information on a plurality of circuits, delay time information on rises and falls of each input terminal and output terminal of said plurality of circuits, and logic operation information representing correspondence between a logical value of each input

terminal and the logical value of the output terminal of said plurality of circuits; and

selecting the delay time between the input terminal and the output terminal of at least one of said plurality of circuits included in the logic circuit as the delay time during the rise or fall of the output terminal of said at least of circuits, according to a logical operation of said at least one of circuits, from the delay time information on the rise and fall of each input terminal and the output terminal of said plurality of circuits, said logical operation being specified by said logical operation information, said delay time information being stored in said library, to perform delay calculation.

4. A computer-readable medium having stored thereon a program for executing:

(a) a process step comprising :

(a1) referencing as library information a delay analysis library containing connection information on a plurality of circuits, delay time information on rises and falls of each input terminal and output terminal of said plurality of circuits, and logic operation information representing correspondence between a logical value of each input terminal and the logical value of the output terminal of said plurality of circuits; and

(a2) selecting the delay time between the input terminal and

the output terminal of at least one of said plurality of circuits included in the logic circuit as a delay time during the rise or fall of the output terminal of said at least of circuits, according to a logical operation of said at least one of circuits, from the delay time information on the rise and fall of each input terminal and the output terminal of said plurality of circuits, said logical operation being specified by said logical operation information, said delay time information being stored in said library; and

(b) a process step of performing delay calculation with said selected delay time as a propagation delay time of said at least one of circuits.